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(71)Applicant : SEIKO EPSON CORP

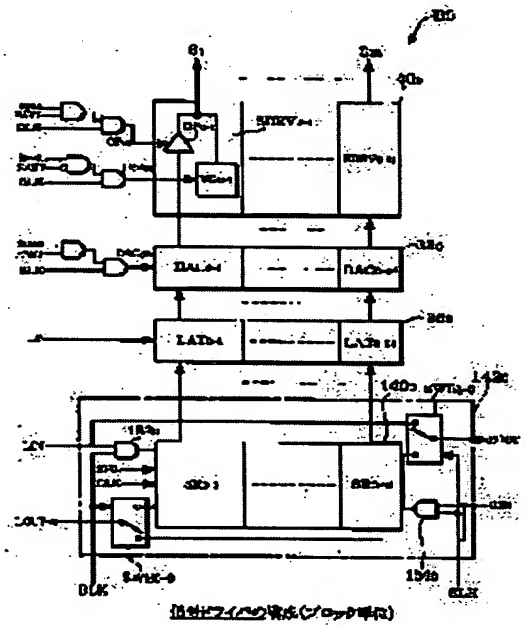
(72)Inventor : MORITA AKIRA

(54) SIGNAL DRIVE CIRCUIT, DISPLAY DEVICE, ELECTRO-OPTICAL DEVICE AND SIGNAL DRIVING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a signal drive circuit which is flexibly adaptive to the change of the size of a panel and realizes a low power consumption, a display device, an electro-optical device and a signal driving method using the signal drive circuit.

SOLUTION: This signal driver (signal drive circuit) includes a shift register 140 shifting successively, by using as a unit a block which is devided for every a plurality of signal lines, image data in accordance with signal lines of the block, a line latch 36 latching the image data in synchronization with a horizontal synchronizing signal LP, a driving voltage generating circuit 38 generating driving voltages based on the image data and a signal line drive circuit 40 and in the driver, high impedance of outputs to the signal lines is controlled based on block output selection data BLK specified in the block unit and, moreover, partial display is controlled based on partial display data PART. The display of the block output selection data is controlled in the block unit in preference to the partial display data PART.



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* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the display which used a signal actuation circuit and this, an electro-optic device, and the signal actuation method.
[0002]
Background Art and Problem(s) to be Solved by the Invention] The liquid crystal panel of various sizes is used by the spread of a portable telephone in recent years or the electronic equipment of another pocket mold. The simple matrix liquid crystal panel using STN (SuperTwisted Nematic) liquid crystal as such a liquid crystal panel and the active matrix liquid crystal panel using thin film transistor (it abbreviates to TFT below Thin Film Transistor:.) liquid crystal are known. By preventing lowering of a frame response with devising the actuation method, the simple matrix liquid crystal panel using STN LCD can prevent lowering of contrast, and can realize low-power-ization. On the other hand, the direction of TFT liquid crystal is suitable for the animation display with the high contrast according [the active matrix liquid crystal panel using TFT liquid crystal] to an original high-speed frame response.
[0003] Generally the actuation circuit which has the signal-line actuation circuit for several line minutes decided with the size of a liquid crystal panel at least is mounted in the electronic equipment carrying such a liquid crystal panel, and optimization of the formation of small lightweight is attained.
[0004] However, the active matrix liquid crystal panel using TFT liquid crystal originates in the complexity of a manufacturing process etc., and a manufacturing cost becomes high compared with the simple matrix liquid crystal panel using STN LCD. And in having carried out the design change of an actuation circuit for every size of a liquid crystal panel, there is a problem of causing the cost high of the product by the increment in a man day, the delay of the commercial-scene charge of a product, etc. increasingly. Furthermore, the active matrix liquid crystal panel using TFT liquid crystal has large power consumption, and it is necessary to attain low-power-ization.
[0005] The place which this invention is made in view of the above technical technical problems, and is made into the object is to offer the signal actuation circuit which can respond to change of panel size flexibly by carrying out actuation control of the signal-line actuation circuit for several line minutes according to the class of panel size, and can attain low-power-ization, the display using this, an electro-optic device, and the signal actuation method.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, this invention a signal line of an electro-optic device which has a pixel specified by two or more scan line and two or more signal lines which cross mutually It is the signal actuation circuit driven based on image data. A horizontal scanning period A line latch who latches image data, and a driver voltage generation means to generate driver voltage for every signal line based on image data latched to said line latch, Based on driver voltage generated by said driver voltage generation means, a signal-line driving means which drives each signal line is included. Said signal-line driving means It is characterized by carrying out high impedance control of the output by making into an unit a block divided for two or

more given signal lines of every.
[0007] Here, you may constitute so that it may have a switching means connected to two or more scan lines where it crosses mutually as an electro-optic device, for example and two or more signal lines and said scan line, and said signal line, and a pixel electrode connected to said switching means.
[0008] Moreover, signal lines divided per block may be two or more signal lines which adjoined mutually, and may be two or more signal lines chosen as arbitration.
[0009] Since it was made to carry out high impedance control of the output of a signal-line driving means by signal actuation circuit which drives a signal line of an electro-optic device based on image data by making into an unit a block divided for two or more given signal lines of every according to this invention, diversification of a class of panel size can also be flexibly provided with an applicable signal actuation circuit. Therefore, a design change of a signal actuation circuit accompanying modification of panel size etc. becomes unnecessary, and low-cost-izing and the early commercial-scene charge can be aimed at.
[0010] Moreover, this invention is characterized by said driver voltage generation means carrying out halt control of operation in said block unit.
[0011] Since it becomes possible to stop actuation of a driver voltage generation means corresponding to a signal line which became unnecessary, in addition to the above-mentioned effect, effective low consumerization is realizable according to this invention, with a class of panel size.
[0012] Moreover, this invention is characterized by including an input change means for sequential connection of the flip-flop corresponding to a signal line being made, bypassing a shift register for once holding image data of 1 horizontal scanning unit latched to said line latch, and a signal line of a block by which high impedance control is carried out, and supplying inputted image data to a flip-flop of the next block one by one.
[0013] Since the block concerned can be bypassed and image data can be supplied to a corresponding signal line even when setting out of a block with which high impedance control of the output was out according to a mounting condition is changed according to this invention, for a supply side of image data, it becomes unnecessary to change image data according to setting out of a block with which high impedance control of the output was carried out, and user-friendliness can be raised for a user.
[0014] Moreover, including a control-lead data-hold means to hold control-lead data in said block unit, based on said control-lead data, this invention is said block unit and is characterized by performing high impedance control of an output of said signal-line driving means, or halt control of said driver voltage generation means of operation.
[0015] Since it was made to perform an output control of a signal-line driving means, or halt control of a driver voltage generation means of operation based on control-lead data which was equipped with a control-lead data-hold means, and was set up per block according to this invention, it can respond to change of a class of panel size easily, and low cost-ization can be attained.
[0016] Moreover, this invention is characterized by carrying out an output control of driver voltage of a signal line to said block unit about 1 or two or more blocks with which high impedance control of the output of said signal-line driving means is not carried out.
[0017] Since it was made to perform an output control of driver voltage of a signal line per block about 1 or two or more blocks with which high impedance control of the output of a signal-line driving means is not carried out according to this invention, a partialness display control by setting out of display area and non-display area becomes possible, and much more low-power-ization can be attained.
[0018] Moreover, 1 by which high impedance control of the output of said signal-line driving means is not carried out, or a signal-line driving means of two or more blocks is characterized by carrying out an output control of driver voltage of a signal line to said block unit based on said partialness indicative data including a partialness indicative-data maintenance means by which this invention holds a partialness indicative data which shows output propriety to a signal line based on image data in said block unit.
[0019] According to this invention, a block divided into a signal actuation circuit which drives a signal line of an electro-optic device based on image data for two or more given signal lines of every is made

into an unit. While making a partialness indicative-data maintenance means to hold a partialness indicative data which shows output propriety to a signal line based on image data have Since it was made to carry out the output control of the image data of 1 horizontal scanning unit per block based on a partialness indicative data specified as this block unit, a partialness display control which can be set as arbitration can be performed. Thereby, power consumption by signal actuation of non-display area is reducible.

[0020] Moreover, an impedance-conversion means, as for this invention, for said signal-line driving means to carry out impedance conversion of the driver voltage generated by said driver voltage generation means, and to output to each signal line, A non-display level voltage supply means to supply given non-display level voltage to said signal line is included. Each signal line of 1 by which high impedance control of the output of said signal-line driving means is not carried out, or two or more blocks Based on said partialness indicative data, it is characterized by driving per block by either among said impedance-conversion means or said non-display level voltage supply means.

[0021] Since it was made to perform either of the supplies of actuation of a signal line based on image data based on an impedance-conversion means, or given non-display level voltage to a signal line by non-display level voltage supply means in a block unit based on a content set as a partialness indicative data according to this invention, non-display area can be set as a given NOMARI color. Thereby, display area set up by partialness display control can be made conspicuous in addition to an effect mentioned above.

[0022] This invention moreover, said impedance-conversion means As opposed to a signal line of a block with which an output was specified as ON by said partialness indicative data A signal line of a block with which impedance conversion of said driver voltage was carried out, it was outputted, and an output was specified by said partialness indicative data off It is made a hi-z state. Said non-display level voltage supply means A signal line of a block with which an output was specified as ON by said partialness indicative data is made into a hi-z state, and it is characterized by supplying given non-display level voltage to a signal line of a block with which an output was specified by said partialness indicative data off.

[0023] According to this invention, based on a partialness indicative data, an impedance-conversion means of a block and a non-display level voltage supply means which were set as non-display area can be controlled per block, and power consumption of a block set as non-display area can be held down effectively.

[0024] Moreover, this invention is characterized by said driver voltage generation means suspending generation actuation of driver voltage for driving a signal line of a block with which an output was specified by said partialness indicative data off.

[0025] According to this invention, based on a partialness indicative data, a driver voltage generation means of a block set as non-display area can be controlled per block, and power consumption of a block set as non-display area can be held down effectively.

[0026] Moreover, as for this invention, said electro-optic device has a pixel electrode prepared through a switching means connected to said scan line and said signal line corresponding to a pixel, and voltage of said non-display level is characterized by being applied voltage of said pixel electrode, and the voltage which makes smaller than a given threshold a voltage difference of said pixel electrode and a counterelectrode prepared through an electro-optics element.

[0027] Applied voltage of a pixel electrode which was prepared through a switching means connected to a scan line and a signal line according to this invention, Since non-display level voltage which makes smaller than a given threshold a voltage difference of this pixel electrode and a counterelectrode prepared through an electro-optics element was set up Non-display area can be set up in the range in which permeability of a pixel of an electro-optic device does not change at least, and simplification of a partialness display control can be attained, without being dependent on precision of partialness non-display level voltage.

[0028] Moreover, as for this invention, said electro-optic device has a pixel electrode prepared through a switching means connected to said scan line and said signal line corresponding to a pixel, and voltage of

said non-display level is characterized by being voltage equivalent to said pixel electrode and a counterelectrode prepared through an electro-optics element.
[0029] Since according to this invention non-display level voltage was set up so that a voltage difference of a pixel electrode and a counterelectrode which counters this might be set to about 0, while attaining simplification of a partialness display control, a foreground color of non-display area is fixed and image display which makes display area conspicuous becomes possible.
[0030] Moreover, this invention is characterized by voltage of said non-display level being either maximum of generable gradation voltage, and the minimum value based on said image data.
[0031] According to this invention, since one side was supplied for either of the voltage of ends of gradation voltage generable [with a driver voltage generation means] as voltage of non-display level, a user can specify a NOMARI color of non-display area as arbitration, and can raise user-friendliness for a user.
[0032] Moreover, this invention is characterized by said block unit being 8 pixel measure.
[0033] According to this invention, setting out of display area and non-display area is attained per character alphabetic character, and simplification of a partialness display control and an image by effective partialness display can be offered.
[0034] moreover, one of electro-optic devices which have a pixel specified by two or more scan line and two or more signal lines which a display concerning this invention intersects mutually, scan actuation circuits which carry out scan actuation of said scan line, and the above which drives said signal line based on image data -- it is characterized by including a signal actuation circuit of a publication.
[0035] According to this invention, even when a class of panel size is changed, the commercial-scene charge of a display which can realize suitable signal-line actuation and reduction of power consumption by low cost can be performed promptly.
[0036] Moreover, this invention is characterized by changing a block which carries out high impedance control of the output of a signal-line driving means of said signal actuation circuit according to relation between arrangement of a signal line of said electro-optic device, and arrangement of a signal-line driving means of said signal actuation circuit.
[0037] According to this invention, since a signal actuation circuit required for actuation of a signal line of an electro-optic device can be arranged in optimal location according to size of an electro-optic device, the versatility of a component side can be raised.
[0038] Moreover, this invention is characterized by said signal actuation circuit carrying out high impedance control of the output of a signal-line driving means arranged near [except the left side edge section and the right side edge section] a center section.
[0039] Since a gap when wiring distance of an electro-optic device and a signal actuation circuit is shortened and these have been arranged can be narrowed according to this invention, cutback-ization of a component-side product can also be attained.
[0040] moreover, one of pixels specified by two or more scan line and two or more signal lines which an electro-optic device concerning this invention intersects mutually, scan actuation circuits which carry out scan actuation of said scan line, and the above which drives said signal line based on image data -- it is characterized by including a signal actuation circuit of a publication.
[0041] According to this invention, even when a class of panel size is changed, the commercial-scene charge of an electro-optic device which can realize suitable signal-line actuation and reduction of power consumption by low cost can be performed promptly.
[0042] Moreover, this invention is characterized by changing a block which carries out high impedance control of the output of a signal-line driving means of said signal actuation circuit according to relation between arrangement of said signal line, and arrangement of a signal-line driving means of said signal actuation circuit.
[0043] Since a signal actuation circuit required for actuation of a signal line of an electro-optic device can be arranged in optimal location according to arrangement of a signal line which specifies a pixel according to this invention, the versatility of a component side can be raised.
[0044] With moreover, a line latch who this invention is a horizontal scanning period and latches image

data A driver voltage generation means to generate driver voltage for every signal line based on image data latched to said line latch, Based on driver voltage generated by said driver voltage generation means, it has a signal-line driving means which drives each signal line. A signal line of an electro-optic device which has a pixel specified by two or more scan line and two or more signal lines which cross mutually It is the signal actuation method of a signal actuation circuit driven based on image data, and is characterized by carrying out high impedance control of said signal-line driving means per block based on control-lead data set as an unit in a block divided for two or more given signal lines of every.
[0045] According to this invention, since high impedance control of the output to a signal line can be carried out per block, it can respond to change of a class of panel size flexibly, and, moreover, low-power-ization can be attained.
[0046]
[Embodiment of the Invention] Hereafter, the gestalt of suitable operation of this invention is explained to details using a drawing.
[0047] 1. Display 1.1 The outline of the configuration of the display which applied the signal actuation circuit (signal driver) in this operation gestalt is shown in the block diagram 1 of a display.
[0048] The liquid crystal equipment 10 as an indicating equipment includes the liquid crystal display (it abbreviates to LCD below Liquid Crystal Display:.) panel 20, the signal driver (signal actuation circuit) (a narrow sense source driver) 30, the scan driver (scan actuation circuit) (a narrow sense gate driver) 50, the LCD controller 60, and a power circuit 80.
[0049] The LCD panel (a wide sense electro-optic device) 20 is formed for example, on a glass substrate. On this glass substrate, the scan lines (a narrow sense gate line) G1-GN (N is the two or more natural numbers) which two or more arrays are carried out in the direction of Y, and are extended in the direction of X, respectively, and the signal-line (narrow sense source line) signal lines S1-SM (M is the two or more natural numbers) which two or more arrays are carried out in the direction of X, and are extended in the direction of Y, respectively are arranged. Moreover, corresponding to the crossing of a scan line Gn (1 <=n<=N and n are the natural number) and signal-line Sm (1 <=m<=M and m are the natural number), TFT22nm (a wide sense switching means) is prepared.
[0050] The gate electrode of TFT22nm is connected to the scan line Gn. The source electrode of TFT22nm is connected to signal-line Sm. The drain electrode of TFT22nm is connected to 26nm of pixel electrodes with a liquid crystal capacity (a wide sense liquid crystal device) of 24nm.
[0051] In the liquid crystal capacity of 24nm, liquid crystal is enclosed and formed between 28nm of counterelectrodes which counter 26nm of pixel electrodes, and permeability changes according to applied voltage inter-electrode [these].
[0052] The counterelectrode voltage Vcom generated by the power circuit 80 is supplied to 28nm of counterelectrodes.
[0053] The signal driver 30 drives the signal lines S1-SM of the LCD panel 20 based on the image data of 1 horizontal scanning unit.
[0054] The scan driver 50 carries out sequential-scanning actuation of the scan lines G1-GN of the LCD panel 20 within a 1 vertical-scanning period synchronizing with a Horizontal Synchronizing signal.
[0055] The LCD controller 60 controls the signal driver 30, the scan driver 50, and a power circuit 80 according to the content set up by hosts, such as a central processing unit (it abbreviates to CPU below Central Processing Unit:.) which is not illustrated. The LCD controller 60 performs supply of the Vertical Synchronizing signal and Horizontal Synchronizing signal which were generated setting out and inside the mode of operation as opposed to the signal driver 30 and the scan driver 50, and, more specifically, supplies polarity-reversals timing of the counterelectrode voltage Vcom to a power circuit 80.
[0056] A power circuit 80 generates a voltage level required for liquid crystal actuation of the LCD panel 20, and the counterelectrode voltage Vcom based on the reference voltage supplied from the outside. Such various voltage levels are supplied to the signal driver 30, the scan driver 50, and the LCD panel 20. Moreover, the counterelectrode voltage Vcom is supplied to the counterelectrode which countered the pixel electrode of TFT of the LCD panel 20, and was prepared.

[0057] Under control of the LCD controller 60, based on the image data supplied from the outside, the signal driver 30, the scan driver 50, and a power circuit 80 cooperate, and such liquid crystal equipment 10 of a configuration carries out display actuation of the LCD panel 20.
[0058] In addition, although he is trying to constitute including the LCD controller 60 to liquid crystal equipment 10, the LCD controller 60 is formed in the exterior of liquid crystal equipment 10, and you may make it constitute it from drawing 1 . Or it is also possible to constitute so that a host may be included in liquid crystal equipment 10 with the LCD controller 60.
[0059] (Signal driver) The outline of the configuration of a signal driver shown in drawing 2 at drawing 1 is shown.
[0060] The signal driver 30 includes a shift register 32, the line latches 34 and 36, the D / A conversion circuit (a wide sense driver voltage generation circuit) 38, and the signal-line actuation circuit 40.
[0061] The shift register 32 has two or more flip-flops, and sequential connection of these flip-flops is made. This shift register 32 will shift the enabling I/O signal EIO to the flip-flop which adjoins one by one synchronizing with a clock signal CLK, if the enabling I/O signal EIO is held synchronizing with a clock signal CLK.
[0062] Moreover, the shift direction change signal SHL is supplied to this shift register 32. As for a shift register 32, the shift direction of image data (DIO) and the I/O direction of the enabling I/O signal EIO are changed by this shift direction change signal SHL. Therefore, flexible mounting can be enabled, without expanding a component-side product by leading about of that wiring, even if it is the case where the locations of the LCD controller 60 which supplies image data to the signal driver 30 according to the mounting condition of the signal driver 30 by changing the shift direction with this shift direction change signal SHL differ.
[0063] As for the line latch 34, image data (DIO) is inputted from the LCD controller 60 for example, per 18 bits (6 bit (gradation data) x3 (RGB each color)). The line latch 34 latches this image data (DIO) with each flip-flop of a shift register 32 synchronizing with the enabling I/O signal EIO by which the sequential shift was carried out.
[0064] The line latch 36 latches the image data of 1 horizontal scanning unit latched by the line latch 34 synchronizing with Horizontal Synchronizing signal LP supplied from the LCD controller 60.
[0065] DAC38 generates the driver voltage analog-ized based on image data for every signal line.
[0066] The signal-line actuation circuit 40 drives a signal line based on the driver voltage generated by DAC38.
[0067] Such a signal driver 30 incorporates the image data of the given unit (for example, 18 bitwises) by which a sequential input is carried out from the LCD controller 60 one by one, and once holds the image data of 1 horizontal scanning unit by the line latch 36 synchronizing with Horizontal Synchronizing signal LP. And each signal line is driven based on this image data. Consequently, the driver voltage based on image data is supplied to the source electrode of TFT of the LCD panel 20.
[0068] (Scan driver) The outline of the configuration of a scan driver shown in drawing 3 at drawing 1 is shown.
[0069] The scan driver 50 includes a shift register 52, level shifters (it abbreviates to last shipment below Level Shifter:.) 54 and 56, and the scan line actuation circuit 58.
[0070] Sequential connection of the flip-flop with which the shift register 52 was formed corresponding to each scan line is made. This shift register 52 will shift the enabling I/O signal EIO to the flip-flop which adjoins one by one synchronizing with a clock signal CLK, if the enabling I/O signal EIO is held to a flip-flop synchronizing with a clock signal CLK. The enabling I/O signal EIO inputted here is a Vertical Synchronizing signal supplied from the LCD controller 60.
[0071] last shipment54 is shifted to the voltage level according to the liquid crystal material of the LCD panel 20, and the transistor capacity of TFT. As this voltage level, since the high voltage level of 20V-50V is needed, for example, a different high resisting pressure process from other logical-circuit sections is used.
[0072] The scan line actuation circuit 58 performs CMOS actuation based on the driver voltage shifted by last shipment54. Moreover, this scan driver 50 has last shipment56, and the voltage shift of output

enable signal XOEV supplied from the LCD controller 60 is performed. On-off control is performed by output enable signal XOEV to which the scan line actuation circuit 58 was shifted by last shipment56.
[0073] Synchronizing with a clock signal CLK, the sequential shift of the enabling I/O signal EIO into which such a scan driver 50 was inputted as a Vertical Synchronizing signal is carried out at each flip-flop of a shift register 52. Since each flip-flop of a shift register 52 is formed corresponding to each scan line, sequential selection of the scan line is alternatively made by the pulse of the Vertical Synchronizing signal held at each flip-flop. The selected scan line is the voltage level shifted by last shipment54, and is driven by the scan line actuation circuit 58. By this, given scan driver voltage will be supplied to the gate electrode of TFT of the LCD panel 20 1 vertical-scanning period. At this time, the drain electrode of TFT of the LCD panel 20 serves as almost equivalent potential corresponding to the potential of the signal line connected to a source electrode.
[0074] (LCD controller) The outline of the configuration of the LCD controller shown in drawing 4 at drawing 1 is shown.
[0075] The LCD controller 60 includes a control circuit 62, random access memory (it abbreviates to RAM below RandomAccess Memory:.) (a wide sense storage means) 64, the host I/O circuit (I/O) 66, and the LCD I/O circuit 68. Furthermore, a control circuit 62 includes the command sequencer 70, the command setting-out register 72, and the control signal generation circuit 74.
[0076] A control circuit 62 performs the signal driver 30, the scan driver 50, various mode-of-operation setting out, a synchronousr control of a power circuit 80, etc. according to the content set up by the host. According to the directions from a host, based on the content set up with the command setting-out register 72, synchronous timing is generated or, more specifically, the command sequencer 70 sets up a given mode of operation to a signal driver etc. in the control signal generation circuit 74.
[0077] RAM64 also becomes the working area of a control circuit 62 while having a function as a frame buffer for performing image display.
[0078] Command data for this LCD controller 60 to control image data, and the signal driver 30 and the scan driver 50 through host I/O66 is supplied. CPU which is not illustrated, and digital-signal-processing equipment (Digital Signal Processor:DSP) or a microprocessor unit (Micro Processor Unit:MPU) is connected to host I/O66.
[0079] Still picture data is supplied from CPU which does not illustrate the LCD controller 60 as image data, or a video data is supplied from DSP or MPU. Moreover, the content of the register for controlling the signal driver 30 or the scan driver 50 and the data for setting up various modes of operation are supplied from CPU which does not illustrate the LCD controller 60 as command data.
[0080] You may make it image data and command data supply data through a respectively separate data bus, and they may common-use-ize a data bus. in this case -- for example, the signal level inputted into the command (CoMmanD:CMD) terminal -- the data on a data bus -- image data -- or by enabling it to identify command data, common use-ization with image data and command data can be attained easily, and cutback-ization of a component-side product is attained.
[0081] The LCD controller 60 holds this image data to RAM64 as a frame buffer, when image data is supplied. On the other hand, when command data is supplied, the LCD controller 60 is held to the command setting-out register 72 or RAM64.
[0082] The command sequencer 70 makes the control signal generation circuit 74 generate various timing signals according to the content set as the command setting-out register 72. Moreover, the command sequencer 70 performs mode setting of the signal driver 30, the scan driver 50, or a power circuit 80 through the LCD I/O circuit 68 according to the content set as the command setting-out register 72.
[0083] Moreover, by the display timing generated in the control signal generation circuit 74, the command sequencer 70 generates the image data of given format from the image data memorized by RAM64, and supplies it to the signal driver 30 through the LCD I/O circuit 68.
[0084] 1.2 When carrying out display actuation of the liquid crystal in time with a reversal actuation method, it is necessary to discharge the charge periodically accumulated in liquid crystal capacity from the endurance of liquid crystal, and a viewpoint of contrast. Therefore, with the liquid crystal equipment

10 mentioned above, reversing the polarity of the voltage impressed to liquid crystal a given period by alternating current-ized actuation is performed. As this alternating current-ized actuation method, there are a frame reversal actuation method and a line reversal actuation method, for example.
[0085] A frame reversal actuation method is a method which reverses the polarity of the voltage impressed to liquid crystal capacity for every frame. On the other hand, a line reversal actuation method is a method which reverses the polarity of the voltage impressed to liquid crystal capacity for every Rhine. In addition, in a line reversal actuation method, its attention is paid to each line, and the polarity of the voltage impressed to liquid crystal capacity with a frame period is reversed.
[0086] Drawing for explaining actuation of a frame reversal actuation method to drawing 5 (A) and (B) is shown. Drawing 5 (A) shows typically the wave of the driver voltage of the signal line by the frame reversal actuation method, and the counterelectrode voltage Vcom. Drawing 5 (B) shows typically the polarity of the voltage impressed to the liquid crystal capacity corresponding to each pixel for every frame, when a frame reversal actuation method is held.
[0087] By the frame reversal actuation method, the polarity of the driver voltage impressed to a signal line as shown in drawing 5 (A) is reversed for every frame period. That is, the voltage VS supplied to the source electrode of TFT connected to a signal line is set to "-V" of negative polarity by the frame f2 of straight polarity "+V" and consecutiveness with a frame f1. The counterelectrode voltage Vcom supplied to the counterelectrode which, on the other hand, counters the pixel electrode connected to the drain electrode of TFT is reversed synchronizing with the polarity-reversals period of the driver voltage of a signal line.
[0088] Since the difference of the voltage of a pixel electrode and a counterelectrode is impressed, as shown in drawing 5 (B), with a frame f1, the voltage of negative polarity will be impressed to liquid crystal capacity by straight polarity and the frame 2, respectively.
[0089] Drawing for explaining actuation of a line reversal actuation method to drawing 6 (A) and (B) is shown.
[0090] Drawing 6 (A) shows typically the wave of the driver voltage of the signal line by the line reversal actuation method, and the counterelectrode voltage Vcom. Drawing 6 (B) shows typically the polarity of the voltage impressed to the liquid crystal capacity corresponding to each pixel for every frame, when a line reversal actuation method is held.
[0091] the polarity of the driver voltage impressed to a signal line by the line reversal actuation method as shown in drawing 6 (A) -- each horizontal scanning period (1H) of every -- and it is reversed for every frame period. That is, the voltage VS supplied to the source electrode of TFT connected to a signal line becomes "-V" of negative polarity by "+straight polarity V" 2H 1H of a frame f1. In addition, the voltage Vs concerned becomes "+V" of straight polarity by "- negative polarity V" 2H 1H of a frame f2.
[0092] The counterelectrode voltage Vcom supplied to the counterelectrode which, on the other hand, counters the pixel electrode connected to the drain electrode of TFT is reversed synchronizing with the polarity-reversals period of the driver voltage of a signal line.
[0093] Since the difference of the voltage of a pixel electrode and a counterelectrode is impressed, as shown in drawing 6 (B), the voltage which polarity reverses for every Rhine will be impressed to liquid crystal capacity with a frame period by reversing polarity for every scan line, respectively.
[0094] Power consumption becomes large although it can generally contribute to improvement in image quality, since the period of change turns into [the way of a line reversal actuation method] a period of one line compared with a frame reversal actuation method.
[0095] 1.3 An example of an actuation wave of the LCD panel 20 of the liquid crystal equipment 10 of a configuration of having mentioned above to liquid crystal actuation wave drawing 7 is shown. Here, the case where it drives with a line reversal actuation method is shown.
[0096] As mentioned above, according to the display timing generated by the LCD controller 60, the signal driver 30, the scan driver 50, and a power circuit 80 are controlled by liquid crystal equipment 10. The LCD controller 60 supplies the polarity-reversals signal POL which shows the Horizontal Synchronizing signal generated inside and reversal actuation timing while carrying out the sequential transfer of the image data of 1 horizontal scanning unit to the signal driver 30. Moreover, the LCD

controller 60 supplies the Vertical Synchronizing signal generated inside to the scan driver 50. Furthermore, the LCD controller 60 supplies the counterelectrode voltage polarity-reversals signal VCOM to a power circuit 80.

[0097] Thereby, the signal driver 30 drives a signal line based on the image data of 1 horizontal scanning unit synchronizing with a Horizontal Synchronizing signal. The scan driver 50 carries out scan actuation of the scan line connected to the gate electrode of TFT arranged in the shape of a matrix at the LCD panel 20 by driver voltage Vg one by one by making a Vertical Synchronizing signal into a trigger. A power circuit 80 supplies the counterelectrode voltage Vcom generated inside to each counterelectrode of the LCD panel 20, performing polarity reversals synchronizing with the counterelectrode voltage polarity-reversals signal VCOM.

[0098] The charge according to voltage with the voltage Vcom of the pixel electrode connected to the drain electrode of TFT and a counterelectrode is charged by liquid crystal capacity. Therefore, image display will become possible if the pixel electrode voltage **** held with the charge accumulated in liquid crystal capacity exceeds the given threshold VCL. If the pixel electrode voltage **** exceeds the given threshold VCL, the permeability of a pixel will change according to the voltage level, and a gradation expression will be attained.

[0099] 2. Signal driver 2.1 The connection relation between the size of the LCD panel 20 and the signal driver 30 in this operation gestalt is typically shown in the high impedance control diagram 8 of a block unit (A), and (B).

[0100] When two or more signal lines extended to Y shaft orientations of the LCD panel 20 are arranged in accordance with X shaft orientations, the signal-line actuation circuit 40 where the signal driver 30 which drives these signal lines generally drives each signal line along the direction of a long side is arranged. Here, when there are more output numbers D of the signal driver 30 than the number N of signal lines of the LCD panel 20, signal-line actuation circuit 94A near [except the left side edge section and the right side edge section] a center section is vacated, and the signal line of the LCD panel 20 and the signal-line actuation circuit of the signal driver 30 are connected with wiring. Since wiring distance can be shortened, the gap of the LCD panel 20 and the signal driver 30 can be narrowed and wiring area 90A can be used effectively by carrying out like this, cutback-ization of a component-side product can also be attained.

[0101] Moreover, in case a signal-line actuation circuit is used only several signal-line minutes according to panel size when the size of the LCD panel 20 is large as shown in drawing 8 (A), high impedance control of the output of signal-line actuation circuit 94A near [except the left side edge section and the right side edge section] a center section is carried out.

[0102] On the other hand, as shown in drawing 8 (B), when the size of the LCD panel 20 is small, high impedance control of the output of signal-line actuation circuit 94B is similarly carried out by arranging the excessive signal-line actuation circuit which increased compared with the case of drawing 8 (A) near [except the left side edge section and the right side edge section] a center section.

[0103] Therefore, the signal driver 30 in this operation gestalt can carry out now high impedance control of the output of the signal-line actuation circuit of the block chosen as arbitration by making into an unit the block divided for two or more given signal lines of every. Then, the signal driver 30 in this operation gestalt has the block output selection register, and holds the block output selection data (a wide sense control-lead data) for setting up whether high impedance control of the output of the signal-line actuation circuit which drives the signal line of each block in a block unit is carried out. Signal actuation of the signal line of the block set as ON with block output selection data will be carried out by the signal-line actuation circuit, and the signal line of the block set up off will be in a hi-z state. therefore, only changing the signal-line actuation circuit which carries out high impedance control of the output -- the size of the LCD panel 20 -- strange -- further -- receiving -- easy -- it can respond -- actuation -- the consumed electric currents accompanying impedance conversion performed in an unnecessary signal-line actuation circuit are reducible. Moreover, it becomes possible to also make the length of each wiring layer connected to the signal line of the LCD panel 20 equate more by arranging the signal-line actuation circuit which carries out high impedance control of the output near [except the left side edge

section and the right side edge section] a center section.
[0104] 2.2 When it is set up so that the output of the signal-line actuation circuit of the block chosen according to the size of the LCD panel 20 to mount may be in a hi-z state as image data carried out bypass input ****, the following problems arise.
[0105] Drawing for explaining the trouble in the case of making the LCD panel 20 display the image for one frame on drawing 9 is shown.
[0106] For example, as shown in drawing 8 , the signal-line actuation circuit 94 near the center section of the signal driver 30 is vacated, and the case where the signal line of the LCD panel 20 and the signal-line actuation circuit of the signal driver 30 are connected by wiring is considered.
[0107] Even if it drives a signal line based on image data 96A for one frame which the user created as opposed to such a signal driver 30, the place which you originally want to display on the LCD panel 20 like image 96B, image 96C will be actually displayed on the LCD panel 20 by the signal-line actuation circuit 94 where the output was made into the hi-z state near the center section, and the non-display area 98 will be formed in the edge of the LCD panel 20 of it.
[0108] That is, if a signal line is driven in the condition that image data is not supplied to the signal-line actuation circuit corresponding to the signal line which image data is supplied to the signal-line actuation circuit 94 corresponding to the signal line which should be supplied, and which does not come out, and should be supplied, it means that the image which a user does not mean will be displayed. Therefore, when displaying such an image on the LCD panel 20, a user needs to recognize the block with which the output was made into the hi-z state, and needs to supply image data to the signal driver 30.
[0109] However, it becomes inconvenience extremely to change the image data which should be supplied for a user according to the mounting condition.
[0110] Then, since the signal driver 30 in this operation gestalt latches the image data of 1 horizontal scanning unit, in case it carries out a sequential shift and incorporates image data, as mentioned above, it bypasses the flip-flop corresponding to the signal line of the block set up so that an output might be in a hi-z state, and shifts image data to the flip-flop corresponding to the scan line of the following block one by one.
[0111] An example of bypass actuation of such image data is shown in drawing 10 (A) and (B).
[0112] For example, when being set up so that high impedance control of the output of each block may not be carried out as shown in drawing 10 (A), in a shift register 32, the sequential shift of the image data incorporated by the signal driver 30 is carried out.
[0113] On the other hand, with this operation gestalt, as shown in drawing 10 (B), the shift register corresponding to the signal line of the block with which high impedance control of the output is carried out is bypassed, and is supplied to the signal line of the block with which high impedance control of the output is not carried out at a shift register.
[0114] By carrying out like this, even when setting out of the block by which high impedance control of the output was carried out according to the mounting condition is changed, it becomes unnecessary for a user to change the image data which should be supplied, and he can offer the user-friendly liquid crystal equipment for a user.
[0115] 2.3 The signal driver 30 in the output-control book operation gestalt of a block unit can perform signal actuation based on image data by making into an unit the block divided for two or more given signal lines of every, and can realize a partialness display now. Therefore, the signal driver 30 has the partialness display selection register, and holds the partialness indicative data which shows the output propriety of each block in a block unit. The block with which the output was set as ON by the partialness indicative data will be set up as display area which performs signal actuation based on image data to the signal line of the block concerned. On the other hand, the block with which the display was set up by the partialness indicative data off will be set up as non-display area to which given non-display level voltage is supplied to the signal line of the block concerned.
[0116] This block is made into 8 pixel measures with this operation gestalt. Here, 1 pixel consists of triplets of an RGB code. Therefore, the signal driver 30 makes 1 block a total of 24 outputs (for

example, S1-S24). Thereby, since the display area of the LCD panel 20 can be set up per character alphabetic character (1 byte), in the electronic equipment which displays a character alphabetic character like a portable telephone, setting out of efficient display area and its image display become possible.
[0117] An example of the partialness display realized by the signal driver in such this operation gestalt to drawing 11 (A), (B), and (C) is shown typically.
[0118] For example, when the signal driver 30 is arranged to the LCD panel 20 so that two or more signal lines may be arranged in the direction of Y as shown in drawing 11 (A), and the scan driver 50 has been arranged so that two or more scan lines may be arranged in the direction of X, as shown in drawing 11 (B), non-display area 100B is set up per block. What is necessary is to drive only the signal line of the block corresponding to the display area 102A and 104A by carrying out like this based on image data.
[0119] It becomes unnecessary or to drive the signal line of the block corresponding to the non-display area 108B and 110B based on image data by setting up display area 106A per block, as shown in drawing 11 (C). Moreover, you may make it set up two or more non-display area or display area in drawing 11 (B) and (C).
[0120] Other examples of a partialness display realized by the signal driver by this operation gestalt to drawing 12 (A), (B), and (C) are shown typically.
[0121] In this case, what is necessary is to drive only the signal line of the block corresponding to the display area 122A and 124A based on image data by setting up non-display area 120B per block, as shown in drawing 12 (B), if the signal driver 30 is arranged to the LCD panel 20 so that two or more signal lines may be arranged in the direction of X as shown in drawing 12 (A), and the scan driver 50 is arranged so that two or more scan lines may be arranged in the direction of Y.
[0122] Or it is not necessary to drive the signal line of the block corresponding to the non-display area 128B and 130B based on image data by setting up display area 126A per block, as shown in drawing 12 (C). In addition, you may make it set up two or more non-display area or display area in drawing 12 (B) and (C).
[0123] Moreover, you may make it each display area divide for example, still picture display area and animation display area. While being able to offer a screen legible for a user by carrying out like this, it becomes possible to attain low-power-ization.
[0124] In the signal driver 30 in this operation gestalt, the signal-line actuation circuit 40 is controlled per block, and drives the signal line of a block by the operational amplifier by which voltage follower connection was made, or the non-display level voltage supply circuit.
[0125] The content of control of the signal-line actuation circuit in this operation gestalt is typically shown in drawing 13 (A), (B), and (C).
[0126] To the signal line of the block set up so that an output might carry out high impedance control with block output selection data (control-lead data), as shown in drawing 13 (A), high impedance control of the output of an operational amplifier which stops generation control of the driver voltage by DAC38A and by which voltage follower connection was both made in signal-line actuation circuit 40A is carried out. And as for the non-display level voltage supply circuit of signal-line actuation circuit high impedance control of the output is carried out.
[0127] Moreover, it is set up so that high impedance control of the output may not be carried out with block output selection data (control-lead data). When driving the signal line of the block corresponding to the display area where the output was set as ON by the partialness indicative data based on image data, as shown in drawing 13 (B) DAC38B is made to generate driver voltage, the operational amplifier by which voltage follower connection was made in signal-line actuation circuit 40B performs impedance conversion, and 1 or two or more signal lines which were assigned to the block concerned are driven. Under the present circumstances, as for the non-display level voltage supply circuit of signal-line actuation circuit 40B, high impedance control of that output is carried out.
[0128] Furthermore, about the signal line of the block corresponding to the non-display area where it was set up in so that high impedance control of the output might not be carried out with block output selection data (control-lead data), and the output was set as OFF by the partialness indicative data, as

shown in drawing 13 (C), high-impedance control is carried out in the output of an operational amplifier which stops generation control of the driver voltage by DAC38C and by which voltage follower connection was both made in signal-line actuation circuit 40C. And 1 or two or more signal lines which were assigned to the block concerned are driven on the non-display level voltage generated by the non-display level voltage supply circuit of signal-line actuation circuit 40C. This non-display level voltage is set as a voltage level which makes smaller than the given threshold VCL whose display the permeability of a pixel changes at least and is attained voltage impressed to the liquid crystal capacity connected to TFT.
[0129]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the outline of the configuration of the indicating equipment which applied the signal actuation circuit (signal driver) in this operation gestalt.
[Drawing 2] It is the block diagram showing the outline of the configuration of a signal driver shown in drawing 1 .
[Drawing 3] It is the block diagram showing the outline of the configuration of a scan driver shown in drawing 1 .
[Drawing 4] It is the block diagram showing the outline of the configuration of the LCD controller shown in drawing 1 .
[Drawing 5] Drawing 5 (A) is the mimetic diagram showing typically the wave of the driver voltage of the signal line by the frame reversal actuation method, and the counterelectrode voltage Vcom. Drawing 5 (B) is the mimetic diagram showing typically the polarity of the voltage impressed to the liquid crystal capacity corresponding to each pixel for every frame, when a frame reversal actuation method is held.
[Drawing 6] Drawing 6 (A) is the mimetic diagram showing typically the wave of the driver voltage of the signal line by the line reversal actuation method, and the counterelectrode voltage Vcom. Drawing 6 (B) is the mimetic diagram showing typically the polarity of the voltage impressed to the liquid crystal capacity corresponding to each pixel for every frame, when a line reversal actuation method is held.
[Drawing 7] It is explanatory drawing showing an example of an actuation wave of the LCD panel of liquid crystal equipment.
[Drawing 8] Drawing 8 (A) and (B) are explanatory drawings showing typically the connection relation between the LCD panel and a signal driver.
[Drawing 9] It is explanatory drawing for explaining the trouble in the case of displaying the image for one frame on the LCD panel.
[Drawing 10] Drawing 10 (A) and (B) are explanatory drawings showing an example of bypass actuation of the image data in this operation gestalt.
[Drawing 11] Drawing 11 (A), (B), and (C) are explanatory drawings showing typically an example of the partialness display realized by the signal driver in this operation gestalt.
[Drawing 12] Drawing 12 (A), (B), and (C) are explanatory drawings showing typically other examples of a partialness display realized by the signal driver in this operation gestalt.
[Drawing 13] Drawing 13 (A), (B), and (C) are explanatory drawings showing typically the content of control of the signal-line actuation circuit in this operation gestalt.
[Drawing 14] Drawing 14 (A) and (B) are explanatory drawings showing typically the signal driver mounted in a different location to the LCD panel.
[Drawing 15] Drawing 15 (A), (B), and (C) are the image data held at the line latch, and explanatory drawing showing the response relation of a block typically.
[Drawing 16] It is the block diagram showing the outline of the configuration of the block unit controlled in the signal driver in this operation gestalt.
[Drawing 17] It is explanatory drawing showing the block output selection register which the signal

driver in this operation gestalt has.
[Drawing 18] It is explanatory drawing showing the partialness display selection register which the signal driver in this operation gestalt has.
[Drawing 19] It is the block diagram showing an example of the configuration of the block data exchange circuit in this operation gestalt.
[Drawing 20] Drawing 20 (A) and (B) are explanatory drawings showing typically an example of actuation of the data bypass circuit in this operation gestalt.
[Drawing 21] Drawing 21 (A) and (B) are explanatory drawings showing typically other examples of actuation of the data bypass circuit in this operation gestalt.
[Drawing 22] It is the block diagram showing an example of the configuration of SR which constitutes the shift register in this operation gestalt.
[Drawing 23] It is explanatory drawing for explaining the gradation voltage generated by DAC in this operation gestalt.
[Drawing 24] It is circuitry drawing showing an example of the configuration of an operational amplifier OP in this operation gestalt by which voltage follower connection was made.
[Drawing 25] It is circuitry drawing showing an example of the configuration of the reference voltage selection-signal generation circuit supplied to the 1st and 2nd differential amplifying circuits of the operational amplifier OP in this operation gestalt by which voltage follower connection was made.
[Drawing 26] It is the block diagram showing an example of the configuration of the non-display level voltage supply circuit in this operation gestalt.
[Drawing 27] It is explanatory drawing showing the content of control of the signal driver in this operation gestalt.
[Drawing 28] It is the timing chart showing an example of a wave of operation of the signal driver in this operation gestalt.
[Description of Notations]
10 Liquid Crystal Equipment (Display)
20 The LCD Panel (Electro-optic Device)
22nm TFT
24nm Liquid crystal capacity
26nm Pixel electrode
28nm Counterelectrode
30 Signal Driver
32, 52, 140, 1400 Shift register
34 36,360 Line latch
38,380 Driver voltage generation circuit (DAC)
40,400 Signal-line actuation circuit
50 Scan Driver
54 56 last shipment
58 Scan Line Actuation Circuit
60 LCD Controller
62 Control Circuit
64 RAM
66 Host I/O
68 LCDI/O
70 Command Sequencer
72 Command Setting-Out Register
74 Control Signal Generation Circuit
80 Power Circuit
100B, 108B, 120B, 128B Non-display area
102A, 106A, 122A, 126A Display area
1420 Data Bypass Circuit

148 Block Output Selection Register
150 Partialness Display Selection Register
1600 Differential Amplifier Section
1620 1st Differential Amplifying Circuit
1640 2nd Differential Amplifying Circuit
1660 1680 Current source
1700 Output Amplifier
1800 Transfer Circuit
1820 Inverter Circuit
1840 XOR Circuit
CLK Clock signal
DACen DAC enable signal
dacen DAC control signal
EIO Enabling I/O signal
LEVen Non-display level voltage supply enable signal
leven Non-display level voltage supply circuit control signal
LP Horizontal Synchronizing signal
OPen Operational amplifier enable signal
open Operational amplifier control signal
POL Polarity-reversals signal
SHL The shift direction change signal
XOEV Output enable signal

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] It is the signal actuation circuit which drives a signal line of an electro-optic device which has a pixel specified by two or more scan line and two or more signal lines which cross mutually based on image data. A horizontal scanning period A line latch who latches image data, and a driver voltage generation means to generate driver voltage for every signal line based on image data latched to said line latch, Based on driver voltage generated by said driver voltage generation means, a signal-line driving means which drives each signal line is included. Said signal-line driving means A signal actuation circuit characterized by carrying out high impedance control of the output by making into an unit a block divided for two or more given signal lines of every.
[Claim 2] It is the signal actuation circuit characterized by said driver voltage generation means carrying out halt control of operation in said block unit in claim 1.
[Claim 3] A signal actuation circuit which sequential connection of the flip-flop corresponding to a signal line is made in claim 1 or 2 , bypasses a shift register for once hold image data of 1 horizontal scanning unit latched to said line latch , and a signal line of a block by which high impedance control is carried out , and is characterized by to include an input change means for supply inputted image data to a flip-flop of the next block one by one .
[Claim 4] A signal actuation circuit characterized by performing high impedance control of an output of said signal-line driving means, or halt control of said driver voltage generation means of operation in said block unit in claim 1 thru/or either of 3 based on said control-lead data including a control-lead data-hold means to hold control-lead data in said block unit.
[Claim 5] A signal actuation circuit characterized by carrying out an output control of driver voltage of a signal line to said block unit in claim 1 thru/or either of 4 about 1 or two or more blocks with which high impedance control of the output of said signal-line driving means is not carried out.
[Claim 6] 1 by which high impedance control of the output of said signal-line driving means is not carried out, or a signal-line driving means of two or more blocks is a signal actuation circuit characterized by carrying out an output control of driver voltage of a signal line to said block unit based on said partialness indicative data including a partialness indicative-data maintenance means to hold a partialness indicative data which shows output propriety to a signal line based on image data to said block unit in claim 5.
[Claim 7] In claim 6 said signal-line driving means An impedance-conversion means to carry out impedance conversion of the driver voltage generated by said driver voltage generation means, and to output to each signal line, A non-display level voltage supply means to supply given non-display level voltage to said signal line, Each signal line of 1 by which high impedance control of the output of an implication and said signal-line driving means is not carried out, or two or more blocks A signal actuation circuit characterized by driving per block by either among said impedance-conversion means or said non-display level voltage supply means based on said partialness indicative data.
[Claim 8] In claim 7 said impedance-conversion means As opposed to a signal line of a block with which an output was specified as ON by said partialness indicative data A signal line of a block with

which impedance conversion of said driver voltage was carried out, it was outputted, and an output was specified by said partialness indicative data off It is made a hi-z state. Said non-display level voltage supply means A signal line of a block with which an output was specified as ON by said partialness indicative data A signal actuation circuit which makes it a hi-z state and is characterized by supplying given non-display level voltage to a signal line of a block with which an output was specified by said partialness indicative data off.

[Claim 9] It is the signal actuation circuit characterized by suspending generation actuation of driver voltage for driving a signal line of a block as which, as for said driver voltage generation means, an output was specified by said partialness indicative data off in claim 7 or 8.

[Claim 10] It is the signal actuation circuit which said electro-optic device has a pixel electrode prepared through a switching means connected to said scan line and said signal line in claim 7 thru/or either of 9 corresponding to a pixel, and is characterized by for voltage of said non-display level to be applied voltage of said pixel electrode, and voltage which makes smaller than a given threshold a voltage difference of said pixel electrode and a counterelectrode prepared through an electro-optics element.

[Claim 11] It is the signal actuation circuit which said electro-optic device has a pixel electrode prepared through a switching means connected to said scan line and said signal line in claim 7 thru/or either of 9 corresponding to a pixel, and is characterized by voltage of said non-display level being voltage equivalent to said pixel electrode and a counterelectrode prepared through an electro-optics element.

[Claim 12] It is the signal actuation circuit characterized by voltage of said non-display level being either maximum of generable gradation voltage, and the minimum value based on said image data in claim 7 thru/or either of 9.

[Claim 13] It is the signal actuation circuit characterized by said block unit being 8 pixel measure in claim 1 thru/or either of 12.

[Claim 14] An electro-optic device which has a pixel specified by two or more scan line and two or more signal lines which cross mutually, a scan actuation circuit which carries out scan actuation of said scan line, and a display characterized by claim 1 which drives said signal line thru/or including a signal actuation circuit of a publication 13 either based on image data.

[Claim 15] A display characterized by changing a block which carries out high impedance control of the output of a signal-line driving means of said signal actuation circuit in claim 14 according to relation between arrangement of a signal line of said electro-optic device, and arrangement of a signal-line driving means of said signal actuation circuit.

[Claim 16] It is the display characterized by carrying out high impedance control of the output of a signal-line driving means arranged near [excluding / on claim 15 and / said signal actuation circuit / the left side edge section and the right side edge section] a center section.

[Claim 17] A pixel specified by two or more scan line and two or more signal lines which cross mutually, a scan actuation circuit which carries out scan actuation of said scan line, and an electro-optic device characterized by claim 1 which drives said signal line thru/or including a signal actuation circuit of a publication 13 either based on image data.

[Claim 18] An electro-optic device characterized by changing a block which carries out high impedance control of the output of a signal-line driving means of said signal actuation circuit in claim 17 according to relation between arrangement of said signal line, and arrangement of a signal-line driving means of said signal actuation circuit.

[Claim 19] A line latch who latches image data a horizontal scanning period A driver voltage generation means to generate driver voltage for every signal line based on image data latched to said line latch A signal-line driving means which drives each signal line based on driver voltage generated by said driver voltage generation means A pixel specified by two or more scan line and two or more signal lines which **** and cross mutually It is the signal actuation method equipped with the above, and is characterized by carrying out high impedance control of said signal-line driving means per block based on control-lead data set as an unit in a block divided for two or more given signal lines of every.

[Translation done.]

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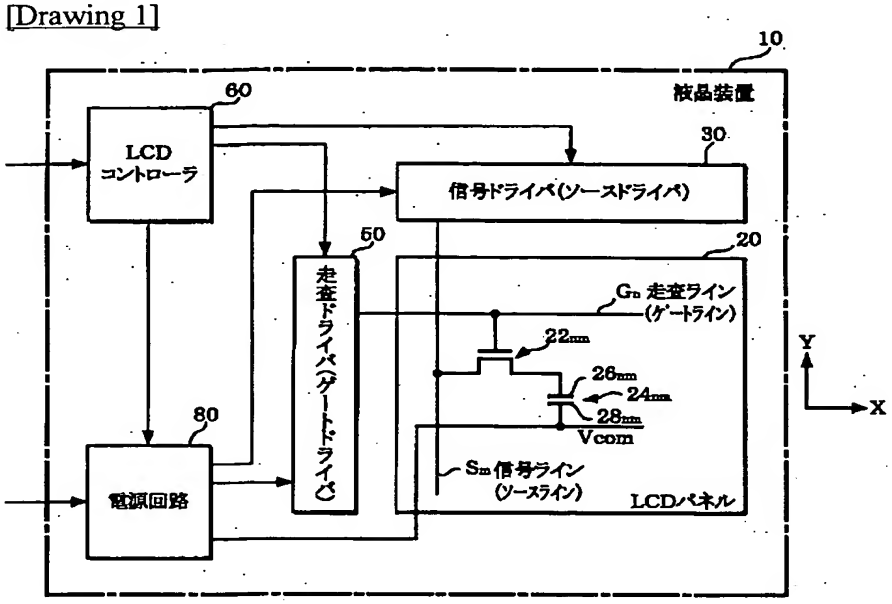
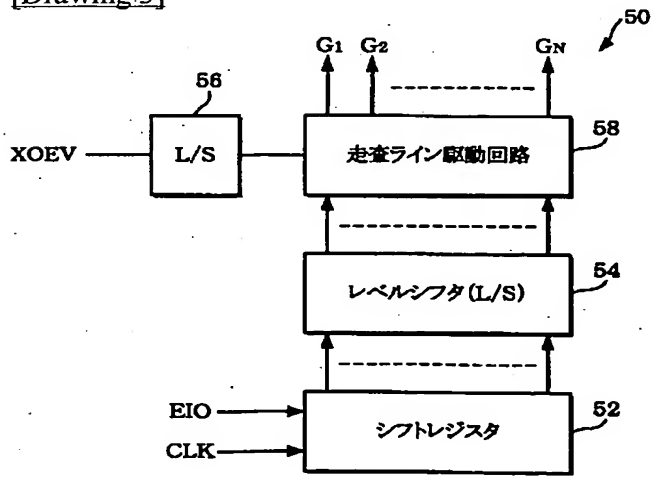
DRAWINGS

[Drawing 1]

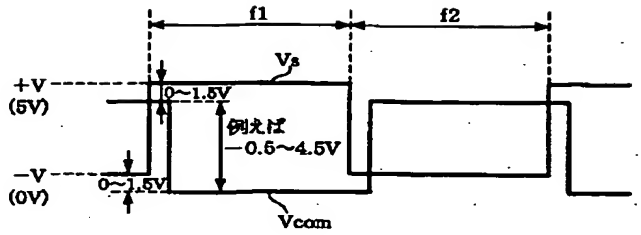


[Drawing 3]

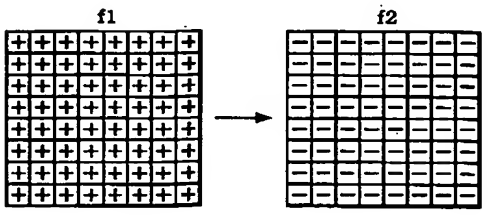


[Drawing 5]

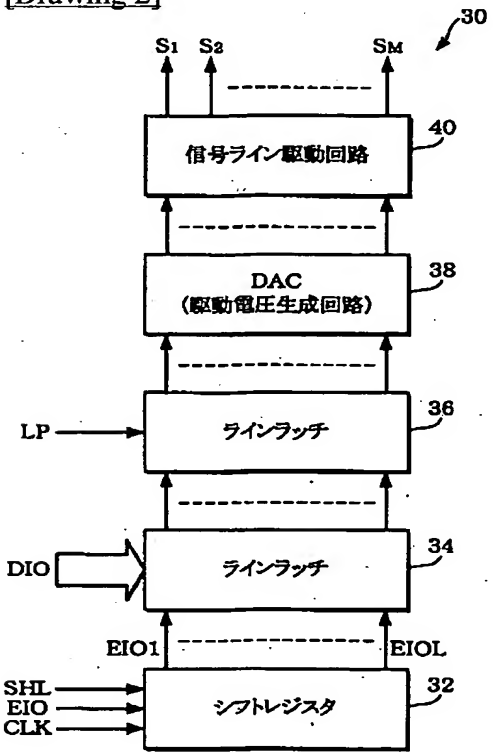
(A)



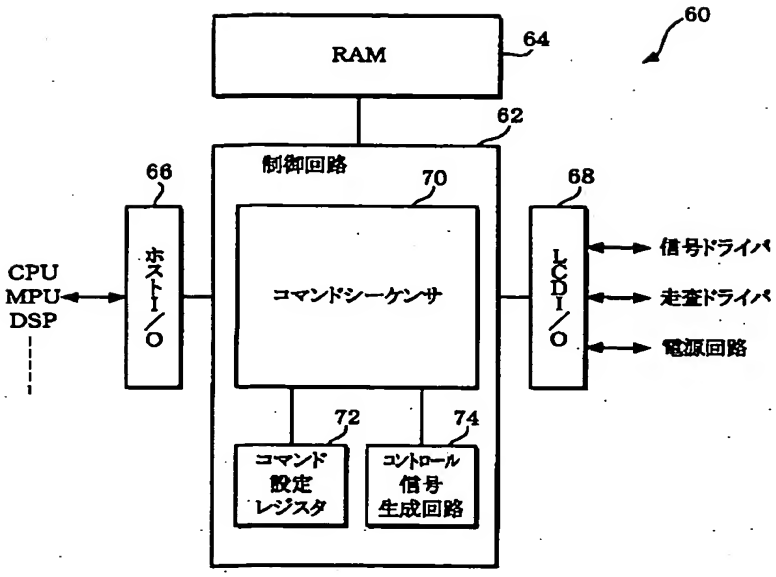
(B)



[Drawing 2]

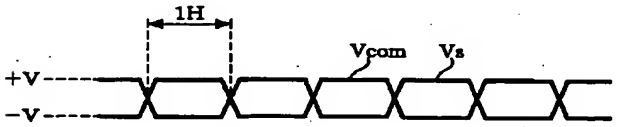


[Drawing 4]

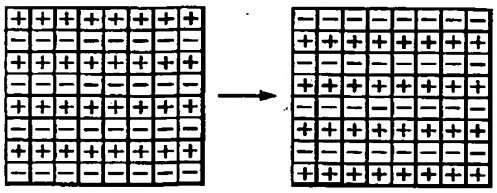


[Drawing 6]

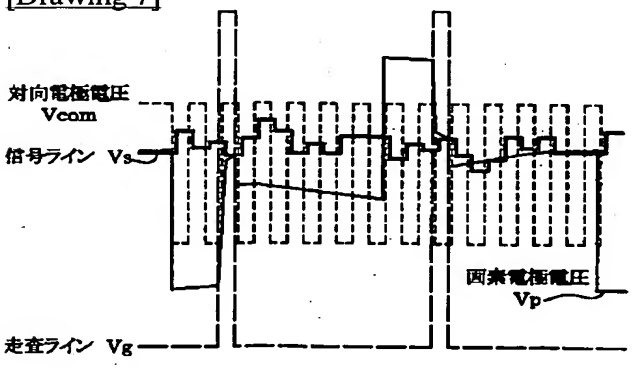
(A)



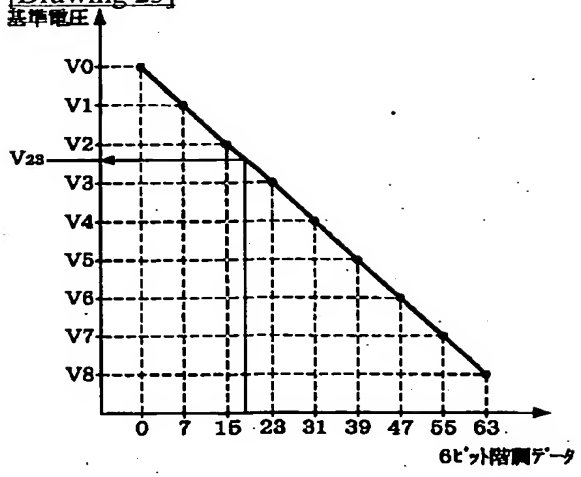
(B)



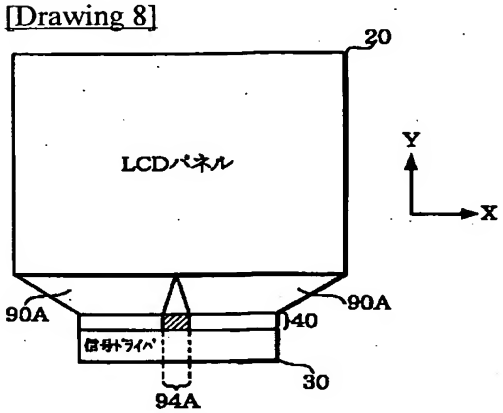
[Drawing 7]



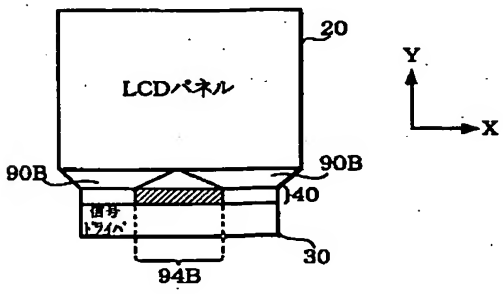
[Drawing 23]



[Drawing 8]

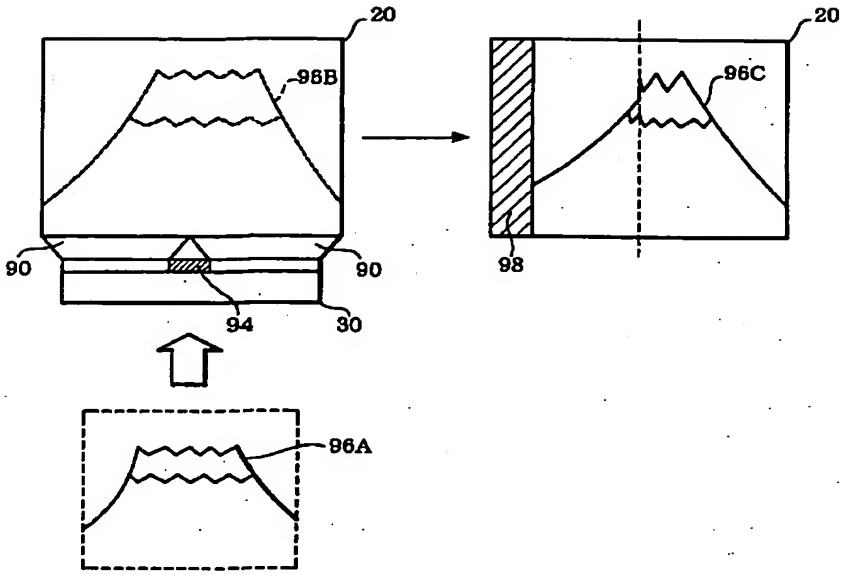


(A) LCDパネルサイズ大



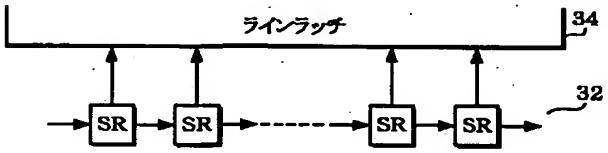
(B) LCDパネルサイズ小

[Drawing 9]

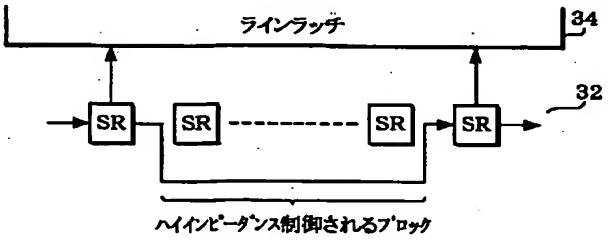


[Drawing 10]

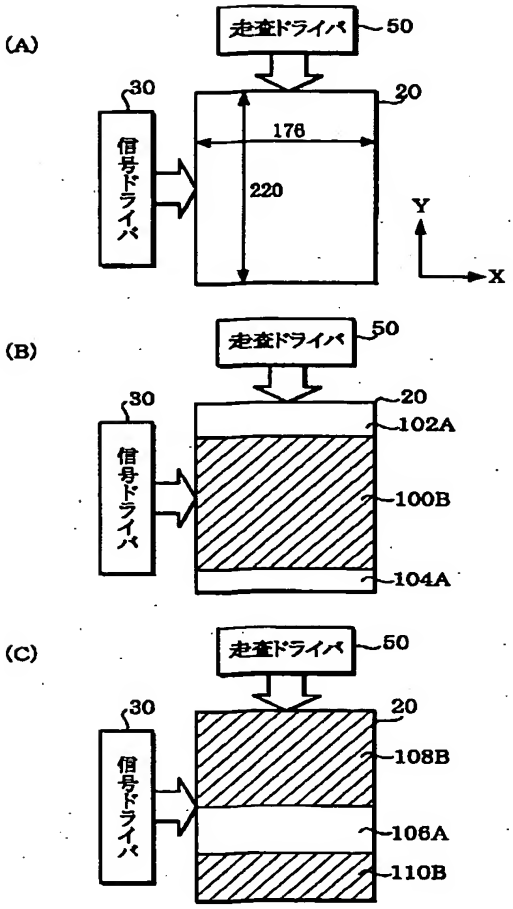
(A)



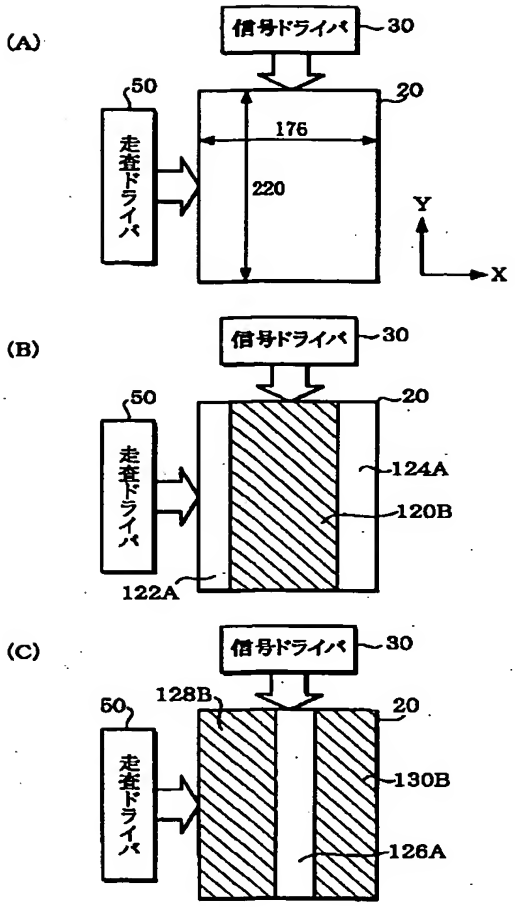
(B)



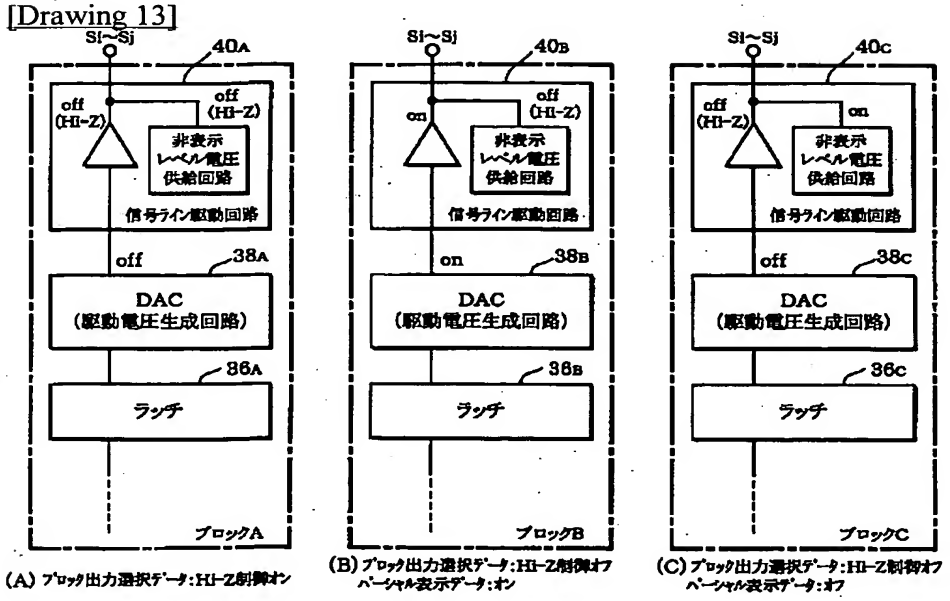
[Drawing 11]


(A)
走査ドライバ
50
30
信号ドライバ
20
176
220
Y
X
(B)
走査ドライバ
50
30
信号ドライバ
20
102A
100B
104A
(C)
走査ドライバ
50
30
信号ドライバ
20
108B
106A
110B

[Drawing 12]

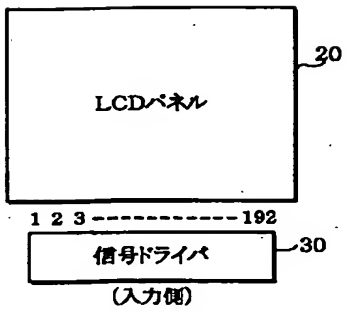


[Drawing 13]

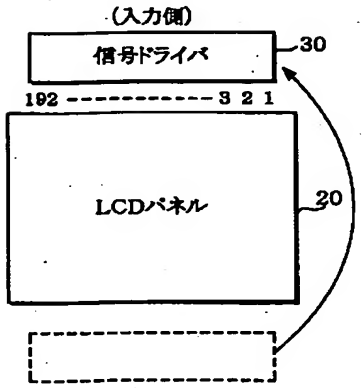


[Drawing 14]

(A)

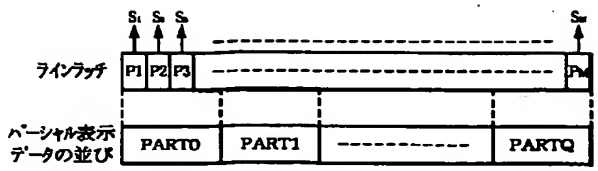


(B)

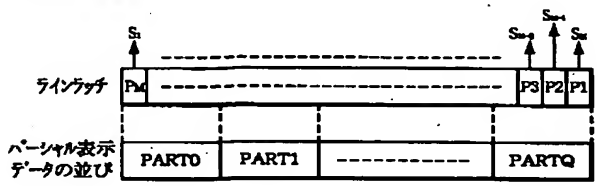


[Drawing 15]

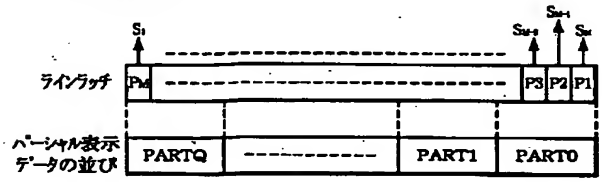
(A) SHL=「H」



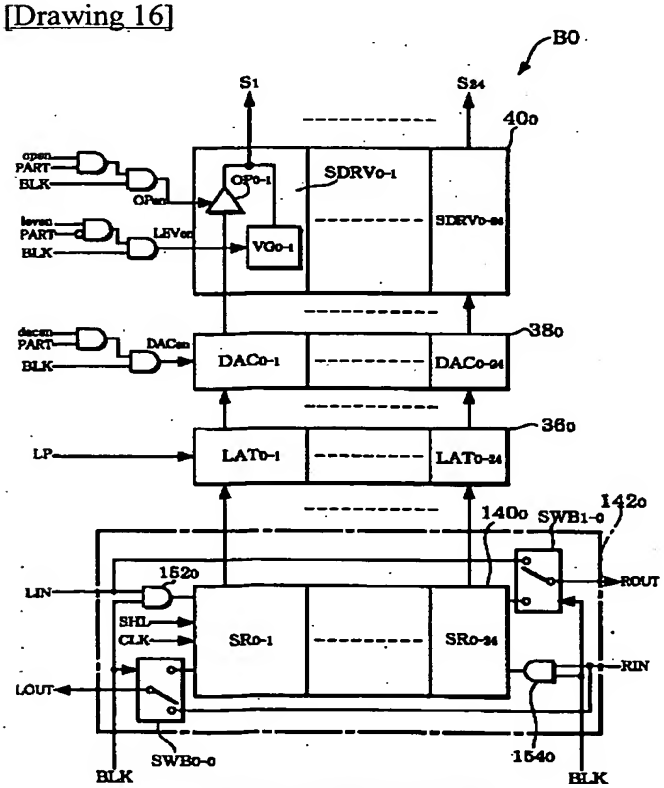
(B) SHL=「L」
データ入れ替えなし



(C) SHL=「L」
データ入れ替えあり

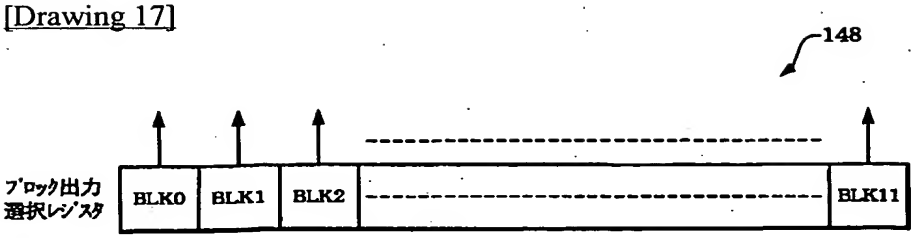


[Drawing 16]

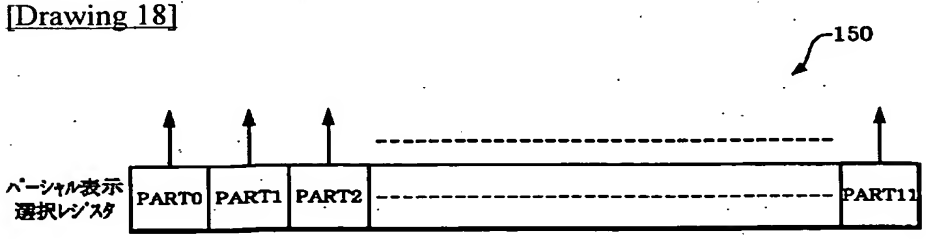


信号ドライバの構成(ブロック単位)

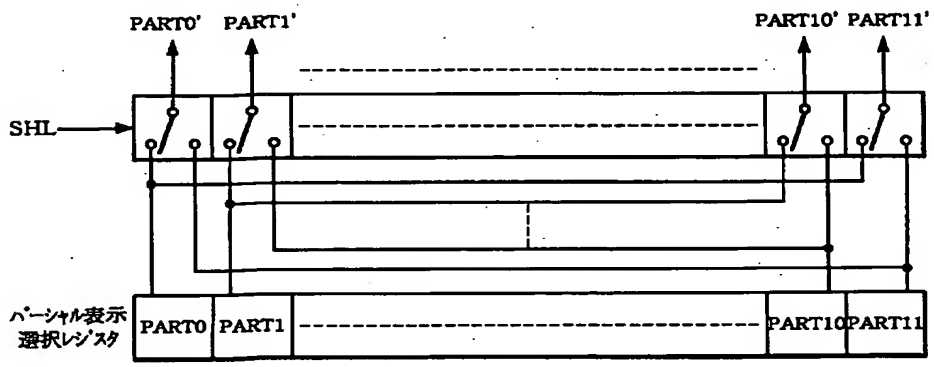
[Drawing 17]



[Drawing 18]



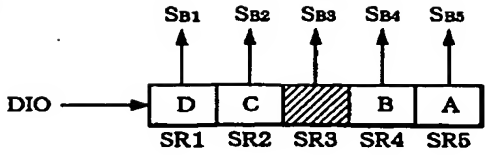
[Drawing 19]



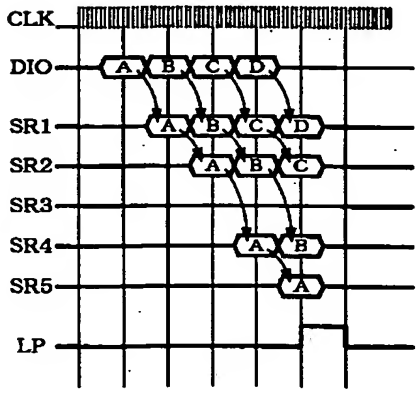
データ入れ替え回路

[Drawing 20]

(A)

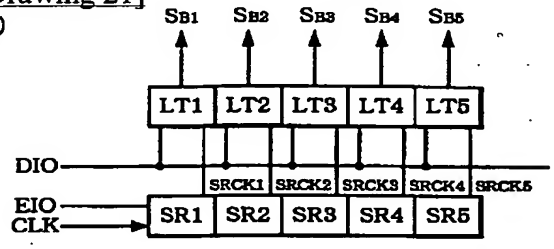


(B)

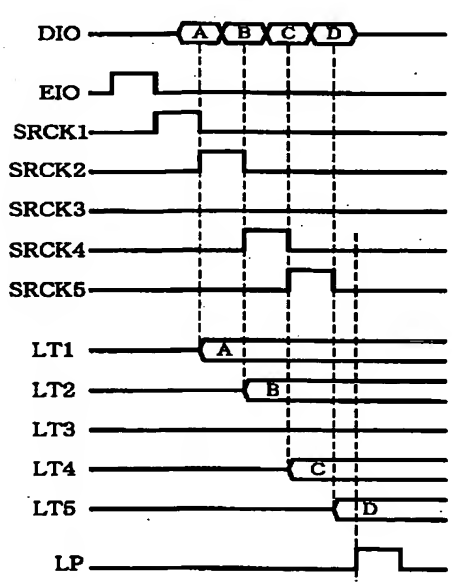


[Drawing 21]

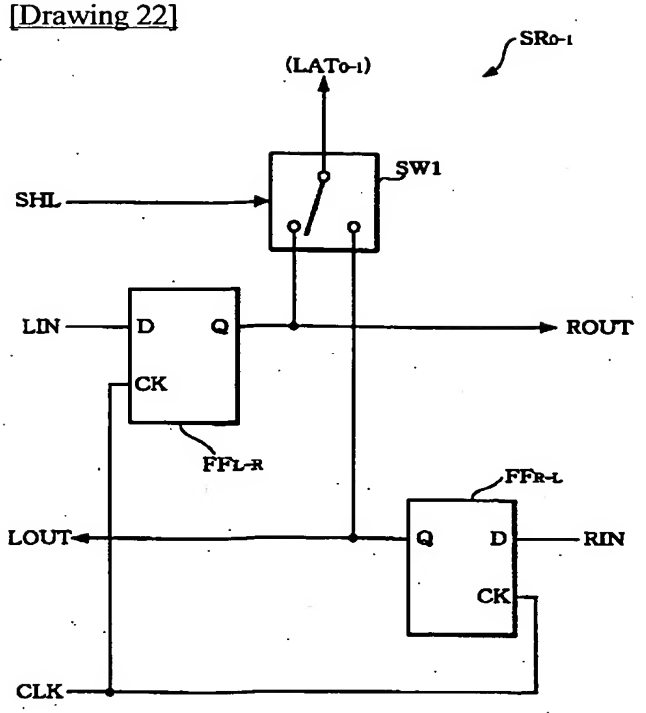
(A)



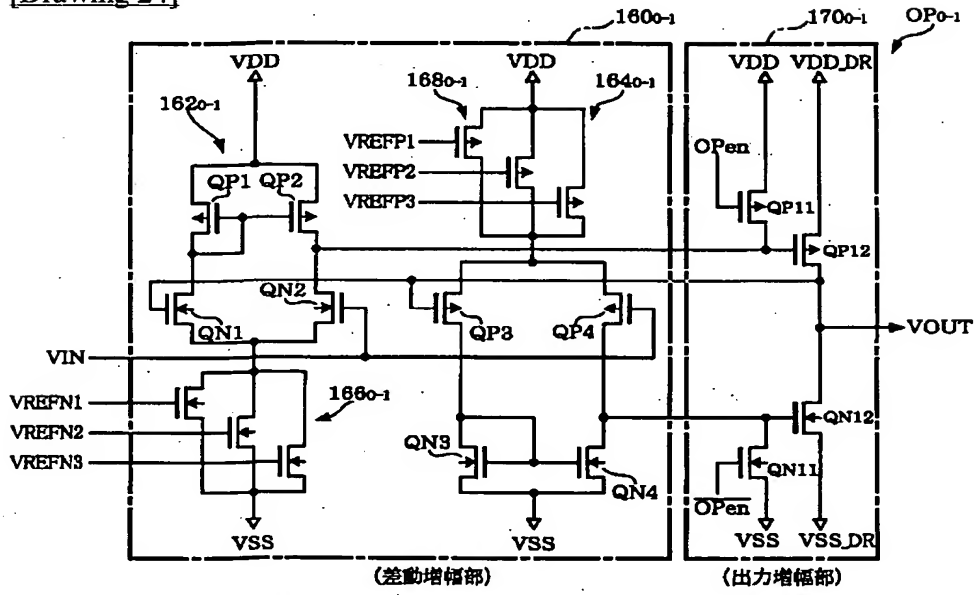
(B)



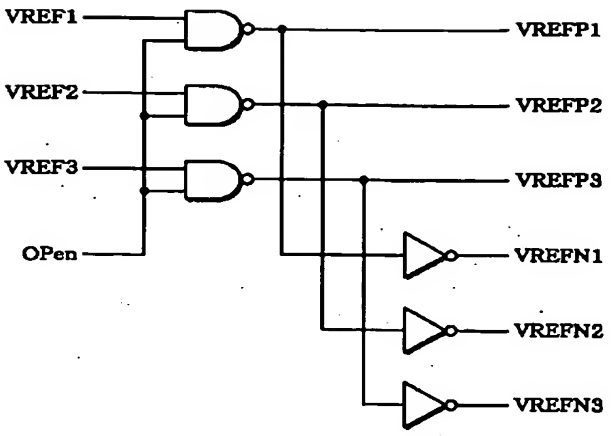
[Drawing 22]



[Drawing 24]

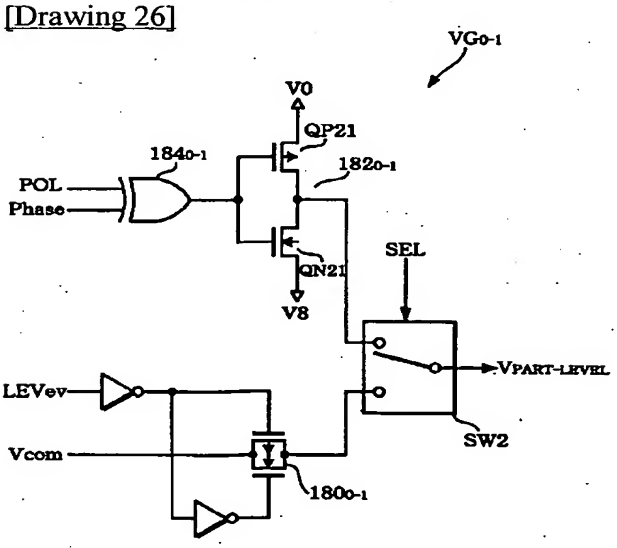


[Drawing 25]



基準電圧選択信号生成回路

[Drawing 26]

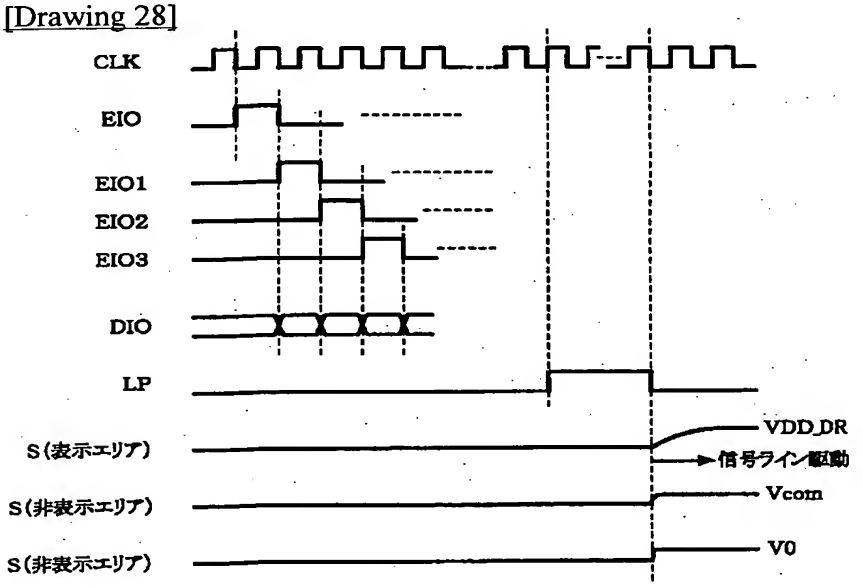


非表示レベル電圧供給回路

[Drawing 27]

ﾌﾞﾛｯｸ出力選択ﾚｼﾞｽﾀ	ﾊﾟｰｼｬﾙ表示選択ﾚｼﾞｽﾀ	ﾃﾞｰﾀﾊﾞｲﾊﾟｽ	DAC	ｵﾍﾟｱﾝﾌﾟ	ﾊﾟｰｼｬﾙ非表示ﾚﾍﾞﾙ出力
ﾌﾞﾛｯｸ出力選択(BLK=1)	ﾊﾟｰｼｬﾙ表示選択(PART=1)	disable	enable	enable	disable
	ﾊﾟｰｼｬﾙ表示非選択(PART=0)	disable	disable	disable	enable
ﾌﾞﾛｯｸ出力非選択(BLK=0)	ﾊﾟｰｼｬﾙ表示選択(PART=1)	enable	disable	disable	disable
	ﾊﾟｰｼｬﾙ表示非選択(PART=0)	enable	disable	disable	disable

[Drawing 28]



[Translation done.]